In Re Patent Application of:
MARINET ET AL.
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In the Claims:

This listing of claims replaces all prior versions and listing of claims in the application.

Claims 1-15 (canceled).

16. (Currently amended) A method of protecting an integrated circuit against piracy, the integrated circuit comprising a central processing unit (CPU) and at least one associated timer, the method comprising:

at the CPU, performing an initialization processing sequence;

at the CPU, detecting the state of the at least one timer after performing the initialization processing sequence and before performing a predetermined processing sequence;

if the at least one timer is not activated, activating the at least one timer and performing the predetermined processing sequence; and

if the at least one timer is activated, disabling the integrated circuit.

17. (Previously presented) The method according to Claim 16, further comprising the CPU deactivating the at least one timer after performance of the predetermined processing sequence.

18. (Previously presented) The method according to Claim 16, further comprising:

the CPU modifying the value of a counter within a protected area in a non-volatile memory if it is detected that the at least one timer is activated;

the CPU comparing the counted value with a predefined threshold; and

the CPU performing a process for protecting confidential data stored within memories in the integrated circuit if the counted value reaches the predefined threshold.

19. (Previously presented) The method according to Claim 18, wherein the protection process comprises erasing the confidential data from the memories in the integrated circuit.

20. (Previously presented) The method according to Claim 18, wherein the protection process comprises erasing a secret code stored within a memory in the integrated circuit.

21. (Previously presented) The method according to Claim 18, wherein the protection process comprises erasing all memories in the integrated circuit.

22. (Previously presented) The method according to Claim 16, wherein the at least one timer comprises a plurality of timers each being associated with a respective authentication calculation of a sequence of a predefined number of calculations; and further comprising:

the CPU detecting the state of a respective timer before performing an associated calculation,

the CPU activating the respective timer if it is not activated; and

the CPU disabling the integrated circuit if the respective timer is activated.

Claims 23-37. (Canceled).

38. (Currently amended) An integrated circuit (IC) comprising:

a central processing unit (CPU); and

at least one timer circuit for protecting the IC against piracy and comprising

a timer which is activated when the IC is powered-on and for a predetermined duration when the IC is powered-off,

a timer activating circuit for activating the timer,

a timer deactivating circuit for deactivating the timer, and

a detection circuit for detecting the state of the timer;

the CPU detecting the state of the timer after performing an initialization processing sequence and before performing a predetermined processing sequence, and, if the timer is not activated, activating the timer and performing the predetermined processing sequence; and

the CPU disabling the IC at predefined times if the timer is in the activated state.

39. (Currently amended) The integrated circuit according to Claim 38, wherein the CPU deactivates the timer

after normal execution of the a predetermined processing sequence.

40. (Previously presented) The integrated circuit according to Claim 38, wherein each timer circuit further comprises:

a power supply detection circuit for detecting a power supply; and

a timer control device for allowing the timer to be activated or deactivated when the power supply is detected during a predetermined time period.

41. (Previously presented) The integrated circuit according to Claim 38, wherein the at least one timer circuit comprises a plurality of timer circuits each being associated with an authentication calculation performed by the CPU; and wherein the CPU determines, before each calculation, the state of the associated timer, and activates the associated timer if it is not activated, and disables the IC if the associate timer is activated.

42. (Previously presented) The integrated circuit according to Claim 38, wherein the at least one timer circuit comprises:

a capacitor;

a discharge circuit associated with the capacitor and designed to discharge over the predetermined duration when the IC is powered-off;

a circuit for detecting capacitor charging;

a capacitor charging control circuit; and

a capacitor discharging control circuit.

43. (Previously presented) The integrated circuit according to Claim 42, wherein the capacitor discharging control circuit discharges the capacitor faster than when the IC is powered-off.

44. (Previously presented) The integrated circuit according to Claim 42, wherein the at least one timer circuit further comprises a MOS transistor associated with the capacitor so that it is only discharged by a leakage current when the IC is powered-off.

45. (Previously presented) The integrated circuit according to Claim 38, further comprising a test circuit for reducing the predetermined duration of the timer during a testing procedure.